JITTER CONTROL PROCESSOR AND A TRANSCEIVER EMPLOYING THE SAME

ABSTRACT OF THE DISCLOSURE

The present invention provides a transceiver couplable to a communications network having a jitter control processor and methods of operating the same. In one aspect of the present invention, the jitter control processor of the transceiver includes a transmitter stage that controls a transmit signal. The transmitter stage includes: (1) a transmit time error measurement system configured to generate a transmit time error signal as a function of timing synchronization associated with a communications network clock and a transceiver master clock, (2) a transmit filter circuit configured to develop a filtered time error signal as a function of the transmit time error signal, and (3) a stuffing control system configured to insert a stuffing control signal into the transmit signal as a function of the transmit time error signal and the filtered time error signal. In another aspect of the present invention, the jitter control processor of the transceiver includes a receiver stage. The receiver stage includes: (1) a receive time error measurement system configured to generate a receive time error signal as a function of a receive clock signal experiencing jitter and a feedback signal, (2) a jitter processing

circuit configured to develop a dejittered control signal as a function of the time error signal, and (3) a clock generator system configured to provide the feedback signal as a function of the dejittered control signal and a transceiver local clock signal.